UTRGV

The University of Texas Rio Grande Valley

College of Engineering and Computer Science

Department of Electrical & Computer Engineering

EECE 3230-02 Electrical Engineering Lab II

Spring 2025

Lab Report 6

Basic RF Circuits

by

Emilio Chavez

Jordan Lara

May 11, 2025

Contents

I.   ABSTRACT

This experiment focused on designing, simulating, and testing three critical radio frequency (RF) circuits: a passive bandpass filter (BPF), a tuned amplifier, and a single balanced mixer. The passive BPF was designed with a target center frequency of 110 kHz and a quality factor (Q) of 50 using a 10 kΩ resistor, 7.23 nF capacitor, and a 289 µH inductor. Simulations and physical measurements were performed to analyze its frequency response, revealing a measured center frequency of 114.5 kHz and a Q of 23.4. The tuned amplifier, constructed using the BPF's LC components and biased for maximum gain, exhibited a center frequency of 126.2 kHz with a measured Q of 10.51. A single-balanced mixer utilizing a CA3086 transistor array was implemented to explore frequency mixing. The single balanced mixer was tested with input signals at 100 kHz (RF) and 10 kHz (LO), generating output harmonics at 90 kHz, 100 kHz, and 110 kHz, verified via FFT analysis. Additional tests at 500 kHz and 1 MHz RF inputs confirmed the mixer's frequency translation capability. Key tests included PSPICE simulations, AC sweeps, frequency response measurements, and FFT-based harmonic analysis. Measured results highlighted deviations from theoretical predictions due to parasitic resistances and component tolerances, emphasizing the challenges of practical RF circuit implementation.

II. BODY

For lab 6, the main objectives are to understand how basic RF circuits work, gain experience using FFT function, gain experience measuring the frequency response of a circuit, and gain experience designing/testing filters.

PART 1: PASSIVE BPF DESIGN AND TEST

For part 1 of Lab 6, it was asked to design and test a passive Band Pass Filer (BPF) using only a resistor Rs, inductor L, and capacitor C. The resistor Rs = 10k Ohms and Q = 50 were given as well as the center frequency f_o = 110 kHz. With Q and center frequency, we can then find the center angular frequency to apply it to that specific bandpass filter's transfer function H(s) by first getting the center angular frequency ω_o which ends up in ω_o = 2*pi*f_o = 2*pi*110k Hz. Now that we have angular center frequency, the following transfer function equation can be applied to find component values for L and C which that equation will be compared to the general transfer function that pertains to that specific circuit which by comparing coefficients, the values of L and C can be found.

System Transfer Function

$$H(s) = \frac{s\left(\frac{\omega o}{Q}\right)}{s^2 + s\left(\frac{\omega o}{Q}\right) + (\omega o)^2}$$

$$H(s) = \frac{s\left(\frac{(2*\pi(110k))}{50}\right)}{s^2 + s\left(\frac{(2*\pi(110k))}{50}\right) + \left(2*\pi(110k)\right)^2}$$

General Transfer Function

$$H(s) = \frac{s\left(\frac{1}{RC}\right)}{s^2 + s\left(\frac{1}{RC}\right) + \frac{1}{LC}}$$

Comparing Coefficients

$$\frac{1}{RC} = \frac{2 * \pi(110k)}{50}$$

$$\frac{1}{(10k)C} = \frac{2 * \pi(110k)}{50}$$

$$C = 7.23 \text{ nF}$$

$$\frac{1}{LC} = \left(2 * \pi(110k)\right)^2$$

$$\frac{1}{L(7.23 \text{ } nF)} = \left(2 * \pi(110k)\right)^2$$

$$L = 289 \text{ μH or } 0.289 \text{ mH}$$

After finding the values for inductance L = 0.289 mH and capacitance C = 7.23 nF, the next step was to find capacitor values that would amount to ~7.23 nF; on the other hand, for inductance, the way to obtain that certain inductance is by making your own inductor using a toroid and wire to give it the amount of turns necessary to get that inductance. To do that the following equation was performed to get the number of turns needed to get that inductance of 0.289 mH:

$$L = AL * N^2$$

$$(0.289mH) = (1270\ nH)N^2$$

N (number of turns) = 15 turns

The next step would be to simulate the circuit on PSPICE, display the circuit schematic, and show how the output behaves as well as display the circuit schematic using parasitic resistances with actual measured values of capacitor C and inductor L as well as display how the output behaves. The schematics and outputs will be displayed below:
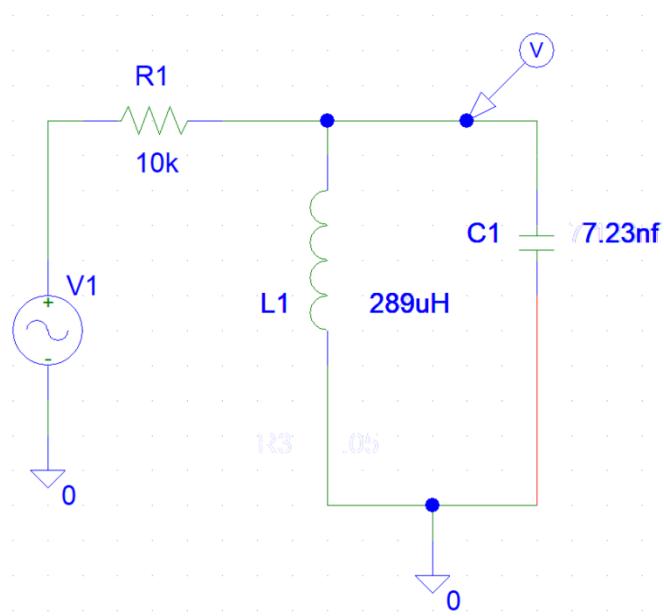

Schematic 1 - Passive BPF Circuit Schematic
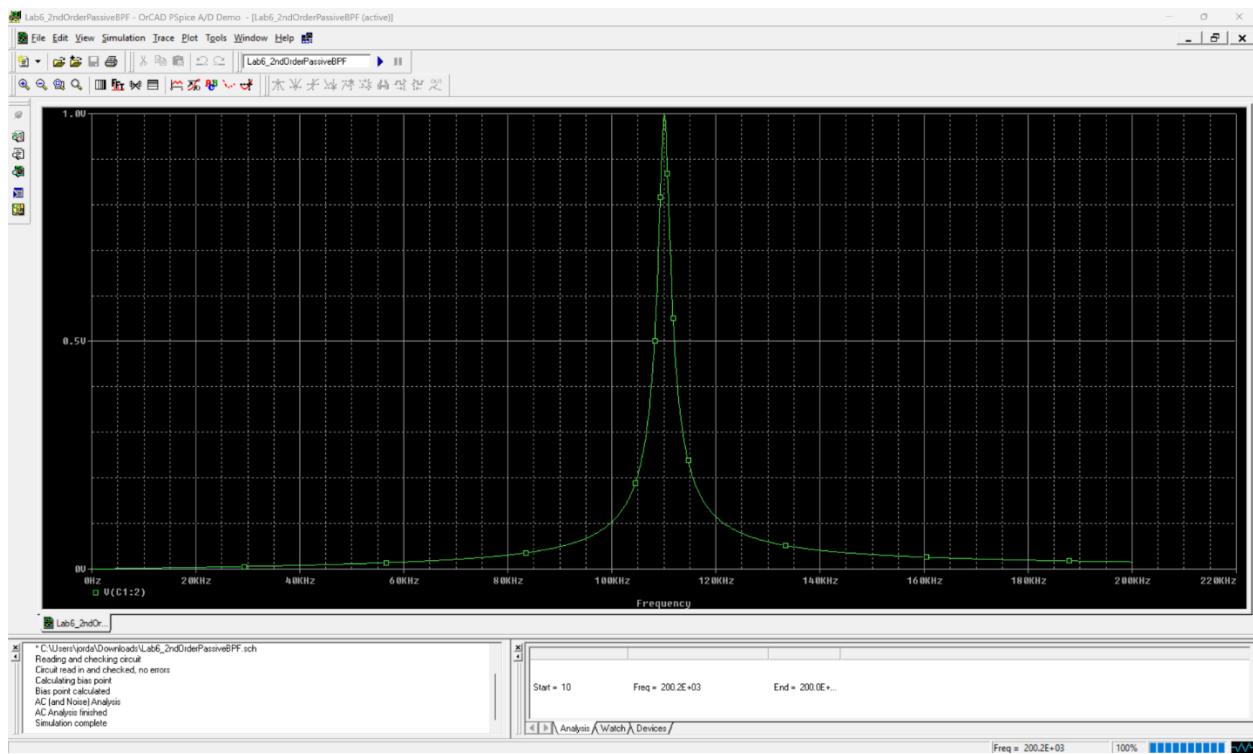
*Simulation 1 - AC Sweep of BPF*
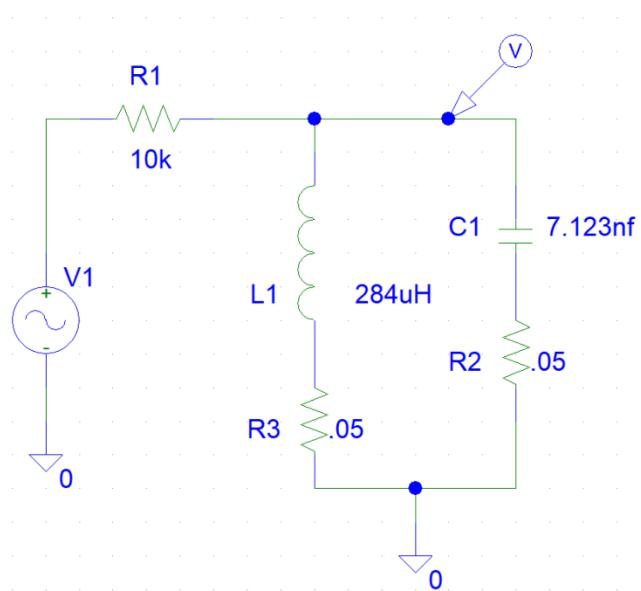
Schematic 2 - BPF Circuit Schematic with Parasitic Resistances
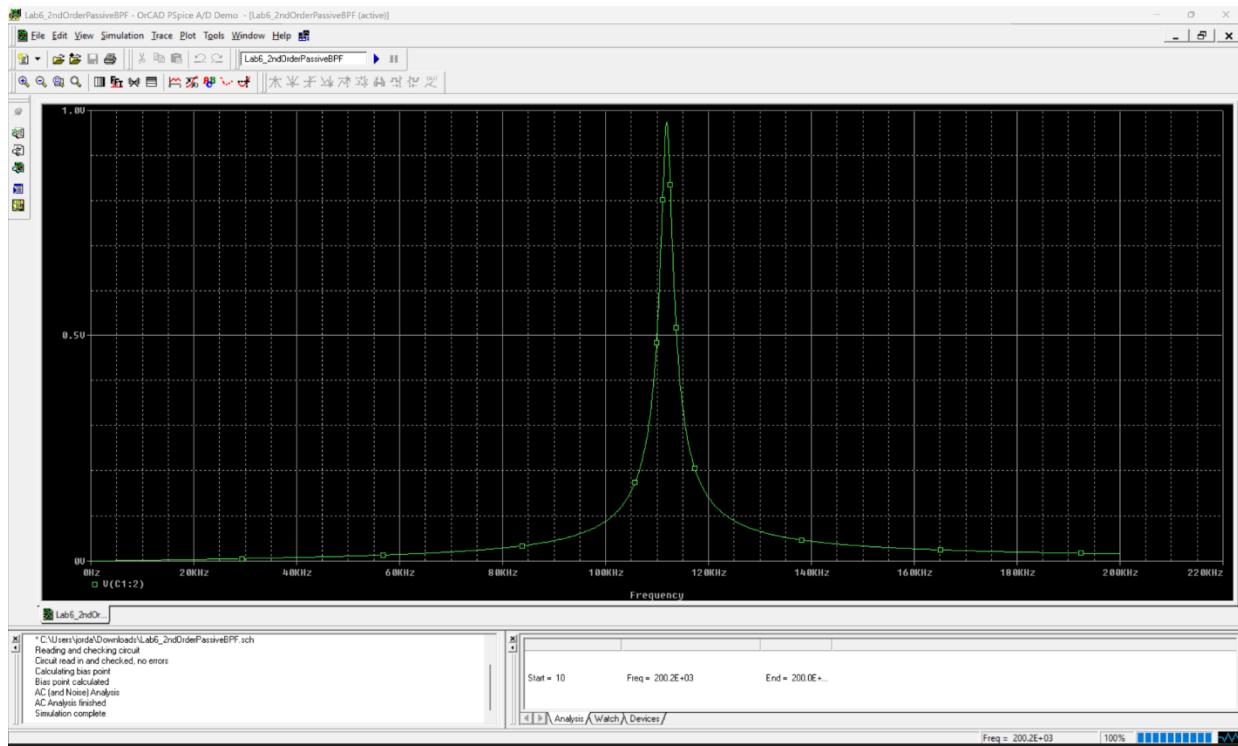
Simulation 2 - AC Sweep of BPF with Parasitic Resistances

After simulating and making sure that the center frequency is correct, implementing the circuit would be the next step and measure the frequency response of the circuit by taking various points of the output/input which will give gain while sweeping the frequency to make sure that the frequency response of the build circuit matches the PSPICE simulation of the simulated frequency response. The following graph displays the measured frequency response with a calculated bandwidth of BW = fH – fL = 117500 – 112600 = 4900 and quality factor Q = f0/(fH – fL) = 114500/(117500 – 112600) = 23.4 (NOTE: fH and fL are obtained by calculating the 3 dB down point of the max gain in decimal and dividing it by square root of 2 which gives the 3 dB down point of 0.69 in our case from a max output of 0.992):
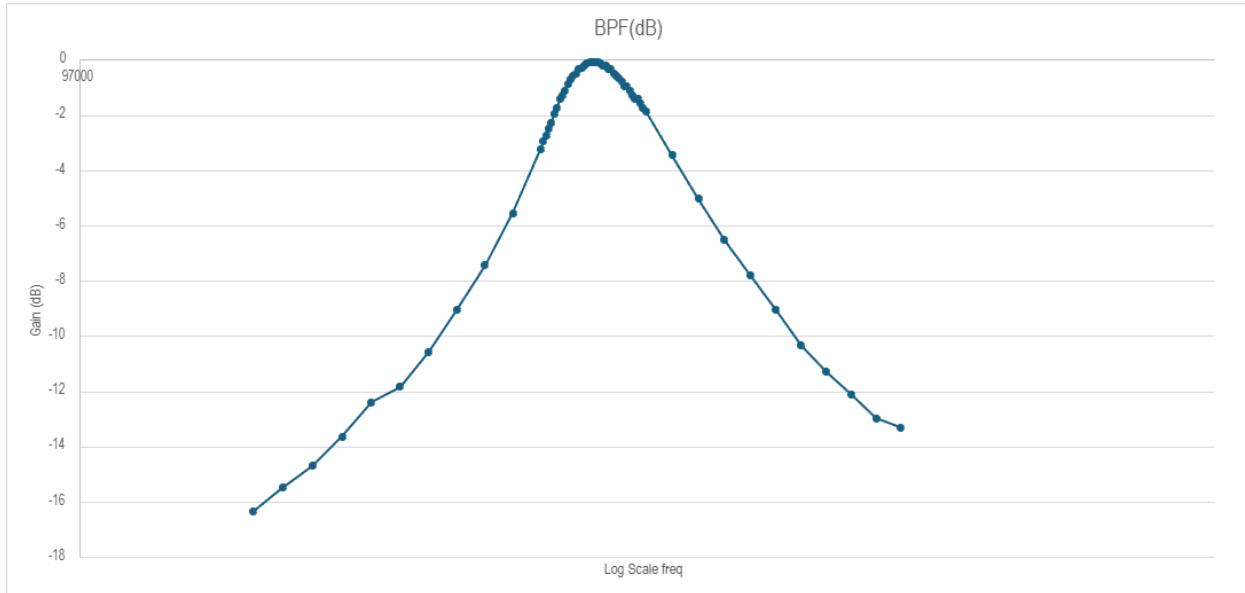
Bode Plot 1 - Frequency Response of Passive BPF Part 1 in dB

PART 2: TUNED AMPLIFIER DESIGN AND TEST

For part 2 of lab 6, it was instructed to build a tuned amplifier and test it using the capacitor and inductor from previous part 1. It was also instructed to build it using +/- 7.5V power supplies and using its common neutral ground to ground the circuit. The missing values using the given circuit schematic would be RB1, RB2, and RC which can be found by picking bias points like current and voltage split, for the other capacitors a capacitance of 47 uF was picked for the source bias capacitor and a capacitor of 0.1 uF was picked for the input capacitance C1. A NMOS 2N7000 was used instead of a BJT because it is easier to work with, so the BJT was swapped with a 2N7000 NMOS. A voltage split of 33/33/33 was picked and a bias current of 100 mA since the 2N7000 can hold up to 200 mA, as a result, 5V was at the drain because of the 1/3rd voltage drop and the remaining voltage was at the source since the voltage drop at RC is 1/3rd of the total 7.5V power supply meaning that 2.5V was dropped across RC

resistor so 2.5V – 0V from ground is 2.5V so there is 2.5V on the source terminal. With these

bias points, the values for RC, RB1 and RB2 can be found using the following equations:

Find RC

$$RC = \frac{V}{I} = \frac{2.5V}{100mA} = 25 \ \Omega$$

Find Gate Voltage using ID equation

$$ID = \frac{kn}{2}(VGS - VT)^2$$

$$100mA = \frac{(0.2)}{2}(VG - 2.5 - 2)^2$$

$$VG = 5.5V \ (ON \ CONDITION) \ or \ 3.5V \ (OFF \ CONDITION)$$

**Find RB1 and RB2 Values by Picking One Resistance**

$$\frac{7.5 - VG}{RB1} = \frac{VG}{RB2}$$

$$\frac{7.5 - 5.5}{RB1} = \frac{5.5}{RB2}$$

$$\frac{RB2}{RB1} = \frac{5.5}{2}$$

Pick RB2 = 55k Ω and RB1 = 20k Ω to make ratio true

After finding all the missing values for RB1, RB2, and RC, the circuit was implemented

and tested to measure its frequency response of the newly built amplifier while taking note of the

center frequency and 3 dB down points to calculate the measured Q. With the measured center

frequency being 126200 Hz, fH being 135000 Hz, fL being 123000 from the voltage 3 dB down

point of 2.24V which gives a bandwidth of BW = 12000 and a quality factor of Q = 10.51. The

following circuit schematic and graph is of the PSPICE simulation followed up with the

measured frequency response graph that was done in excel which all will be shown below:
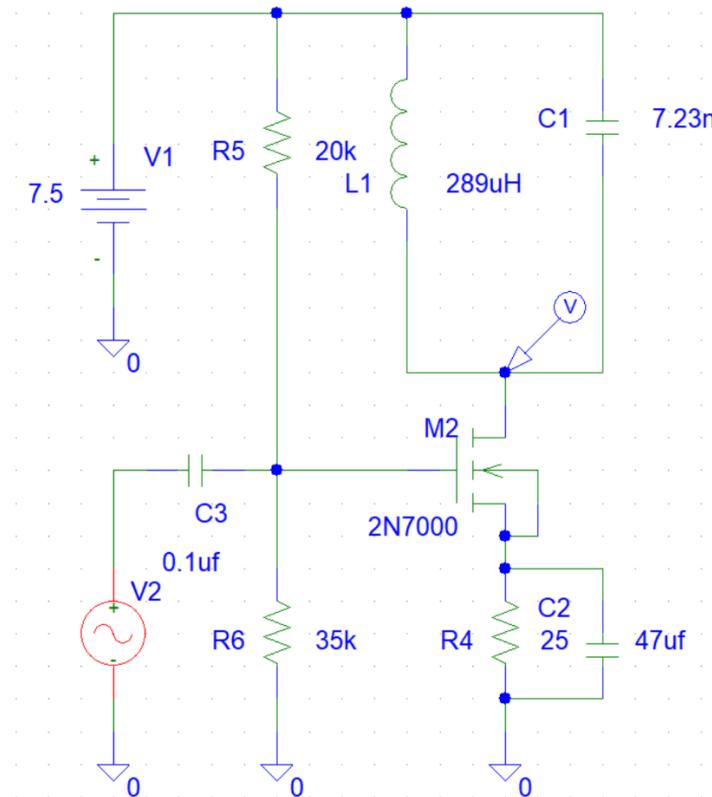
*Schematic 3 - Tuned Amplifier Circuit Schematic*
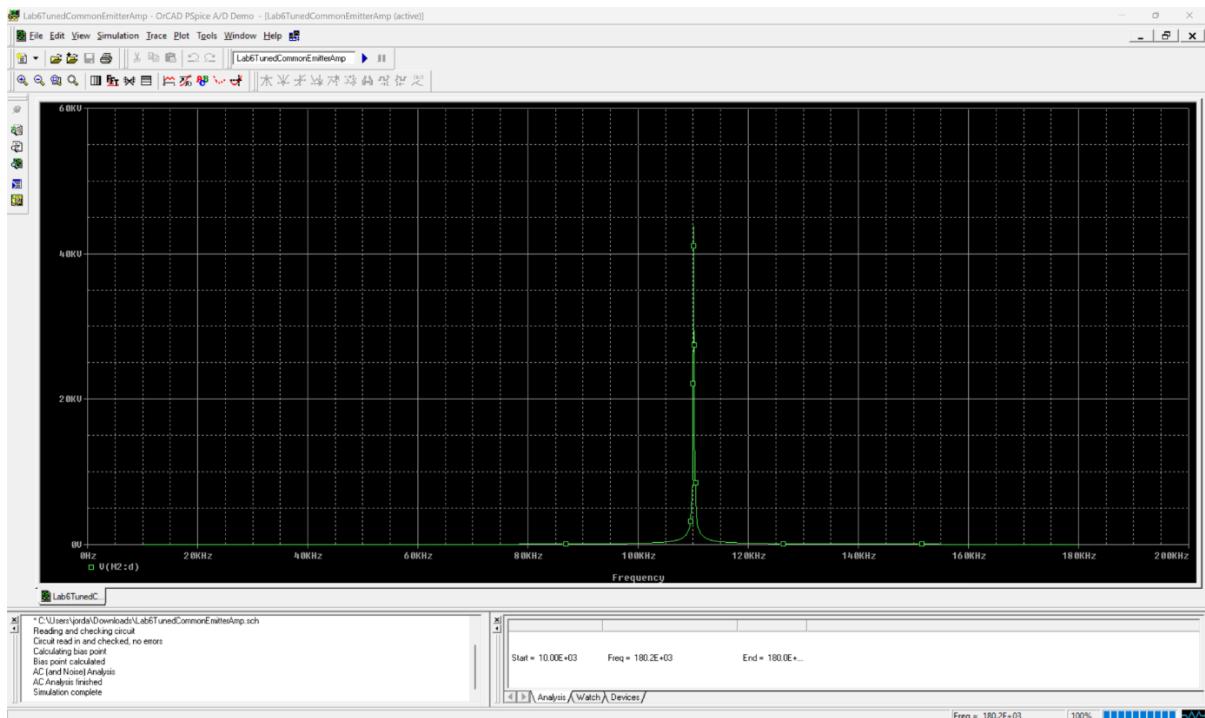
*Simulation 3 - AC Sweep of Tuned Amplifier*
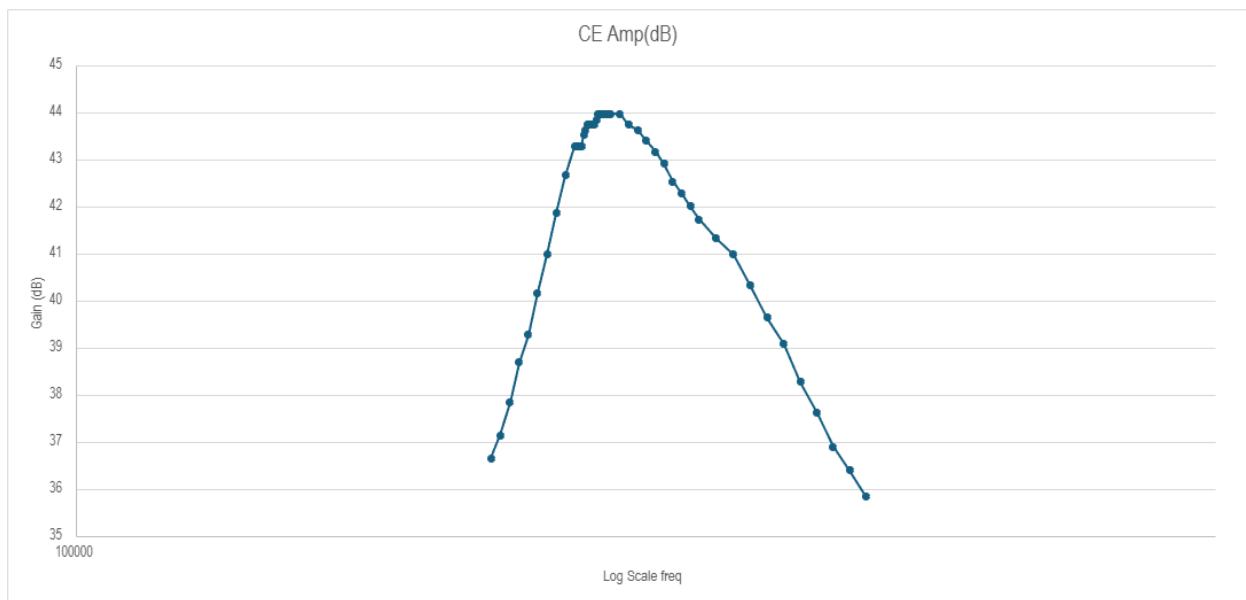
Bode Plot 2 - Frequency Response of Tuned Amplifier Part 2

PART 3: SINGLE BALANCED MIXER

For part 3, it was instructed to build a single balanced mixer which uses two function generators with VRF being the message signal and VLO being the carrier signal. The circuit uses three BJTs which must come from the same substrate chip for Q1 and Q2 to be "equally matched" which means that their transistor dimensions are the "same" and their Kn values are the same. It was recommended to make the bias current around 5 mA. The top resistors RL were picked to be 200 Ω with the RBias2 resistors being 10 kΩ for both, RBias1 resistors being 100 Ω for both, and a RE resistance of 760 Ω. With these resistances, the following circuit schematic was used along with its output which looks like a sine wave within a sine wave which the schematic was used to implement and test on breadboard.
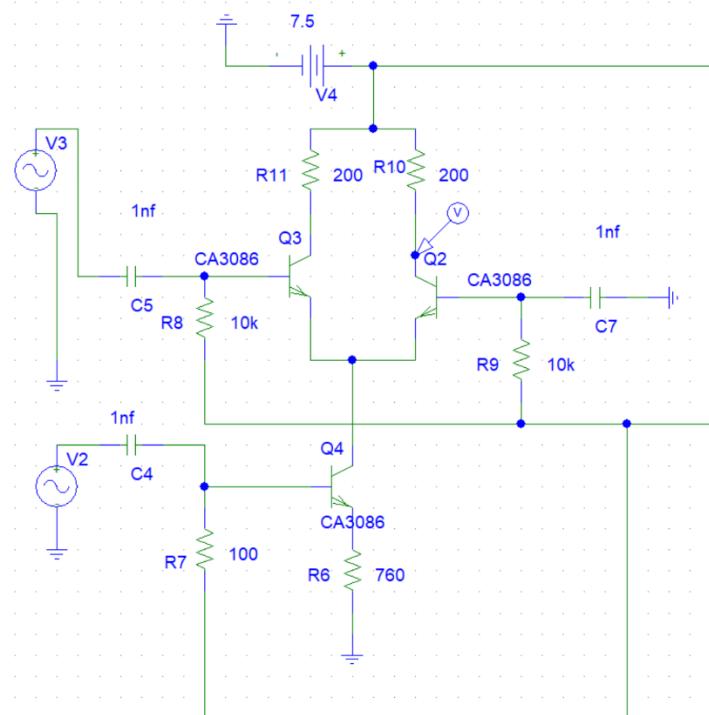

Schematic 4 - Single Balanced Mixer Circuit Schematic
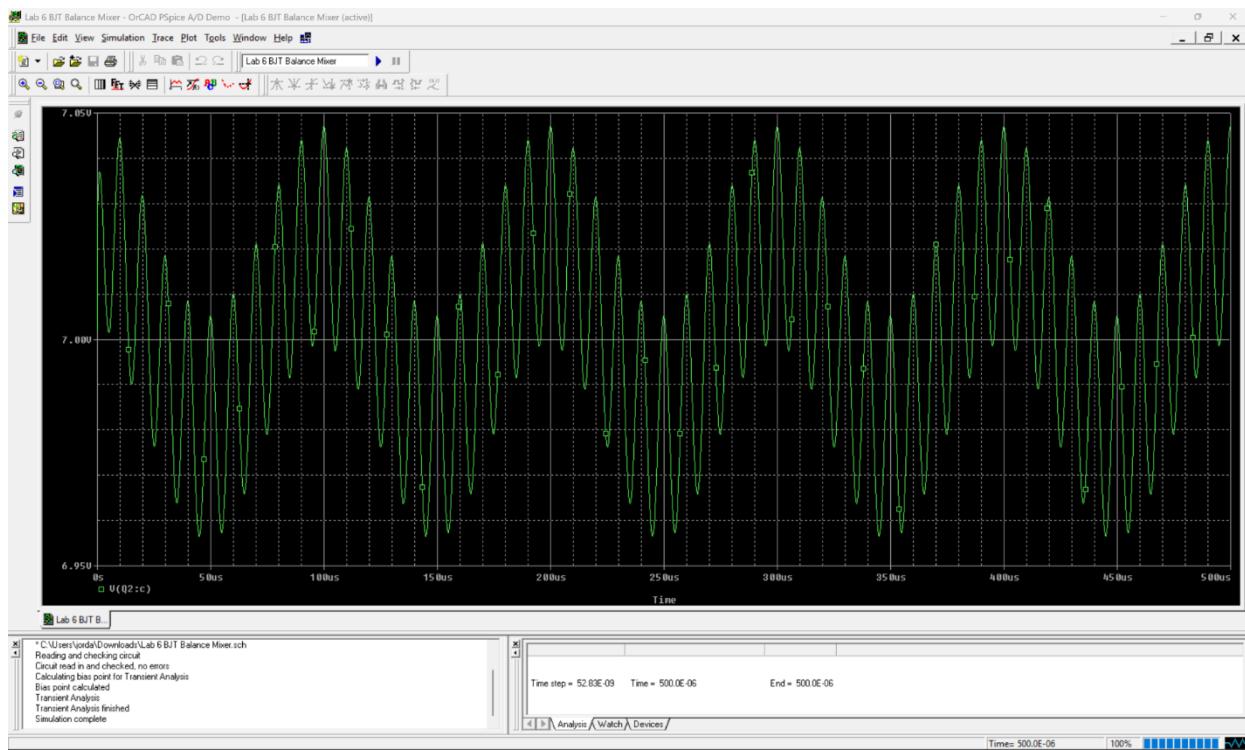
Simulation 4 - AC Sweep of Single Balanced Mixer

To test the circuit, it was asked to feed a 100 kHz sine wave into the VRF port and a 10 kHz sine wave into the VLO port, with an amplitude of 50 mV and 500 mV respectively. The FFT function was used to measure all the significant harmonics present at the mixer's output which display the frequency at f_{rf}, $f_{rf} + f_{LO}$, and $f_{rf} - f_{LO}$ which should display 100 kHz, 110 kHz, and 90 kHz (NOTE: the mixer has two outputs but only one is used). The following FFT scope shots from the oscilloscope display the harmonics at 100 kHz, 110 kHz, and 90 kHz.

Scope Shot 1 - Harmonics at 90k Hz and 100k Hz Using Cursor Function

Scope Shot 2 - Harmonics at 100k Hz and 110k Hz Using Cursor Function
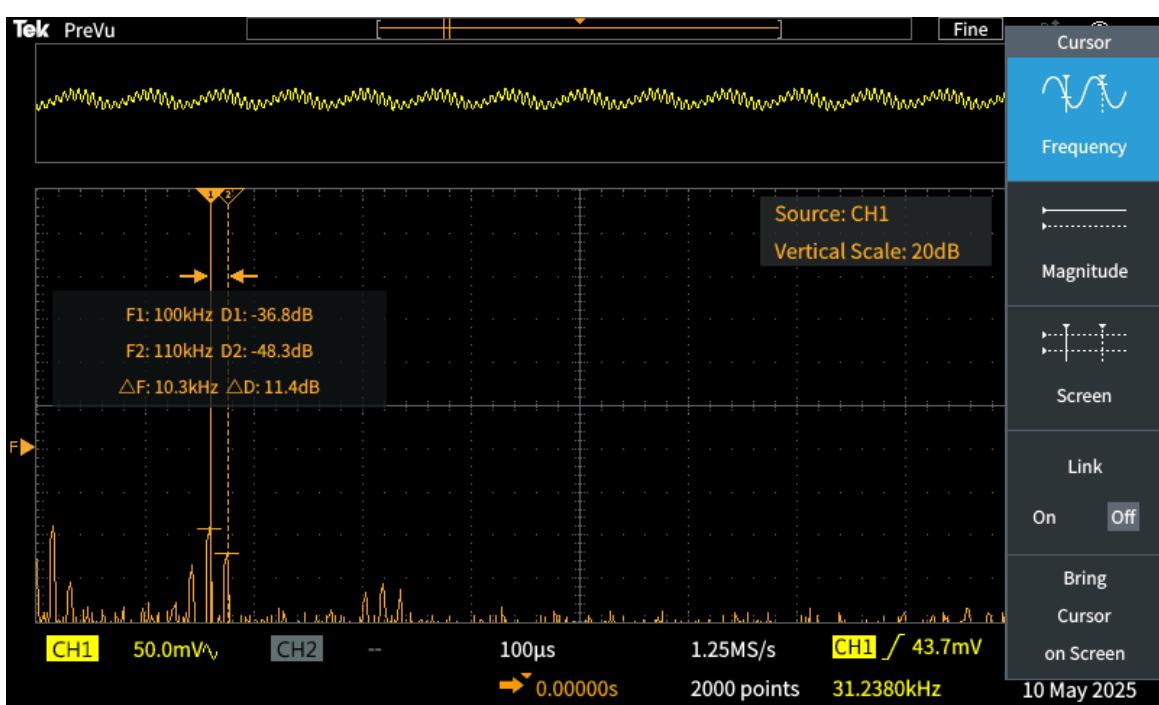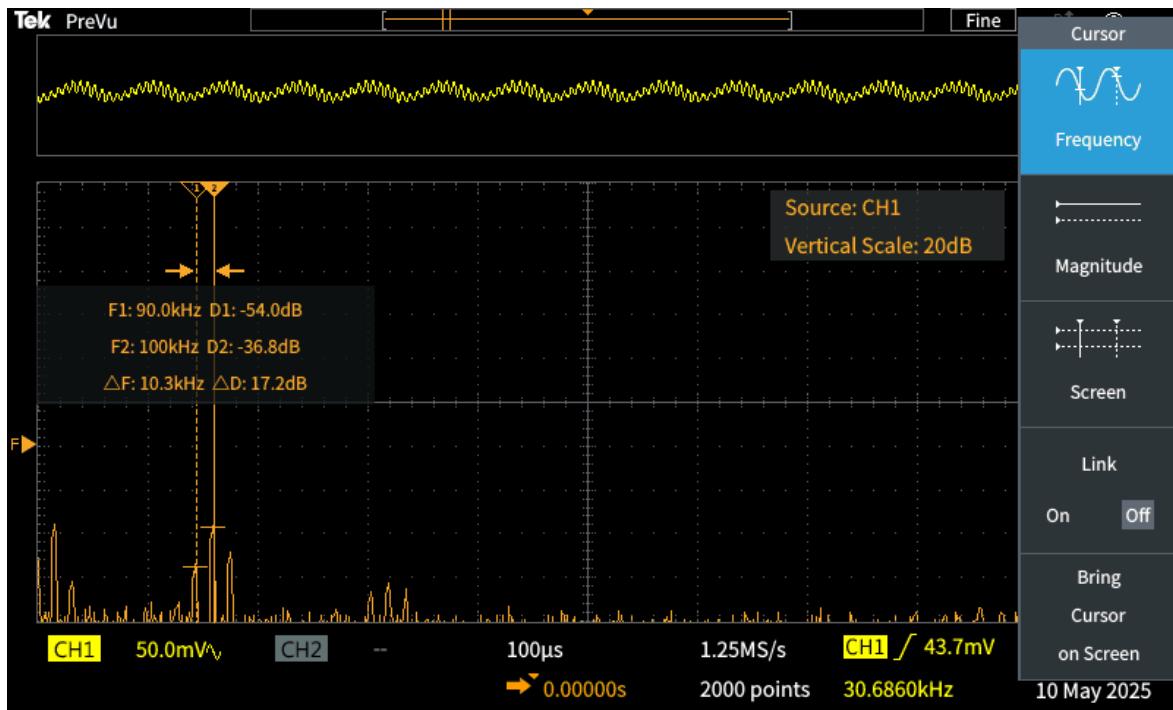
The following scope shots display the periods of VOL and VRF at the mixer's output signal:
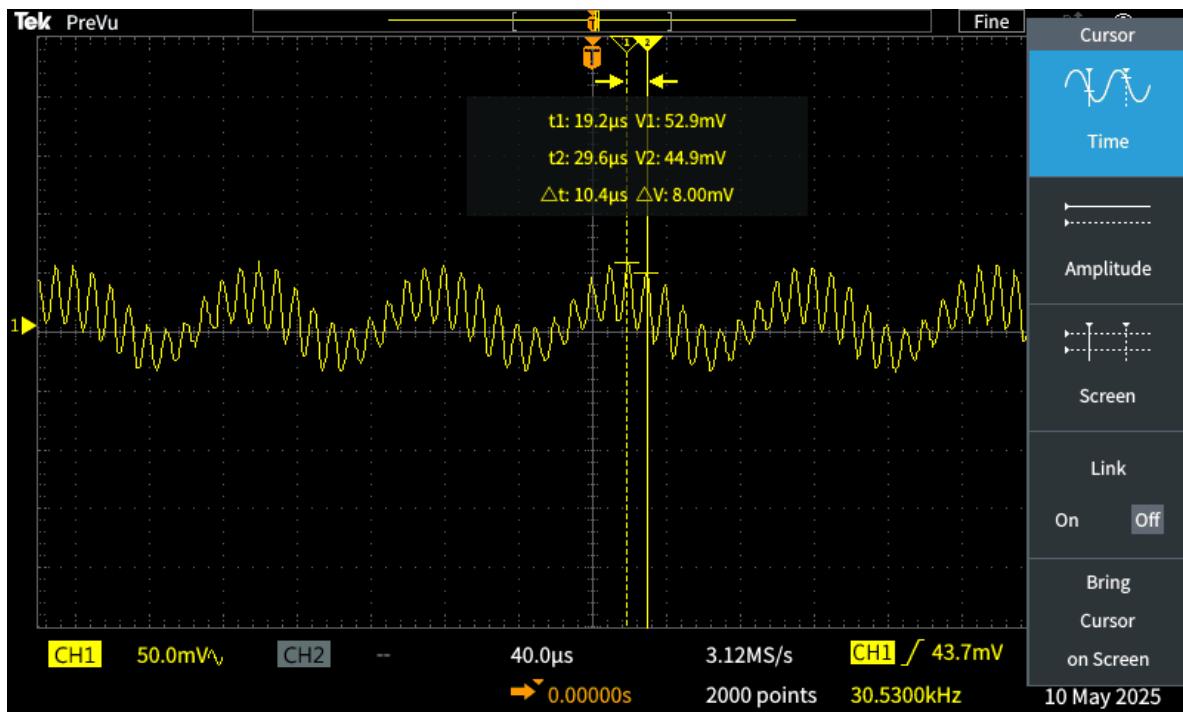
Scope Shot 3 - VOL Period Measured at the Mixer's Output
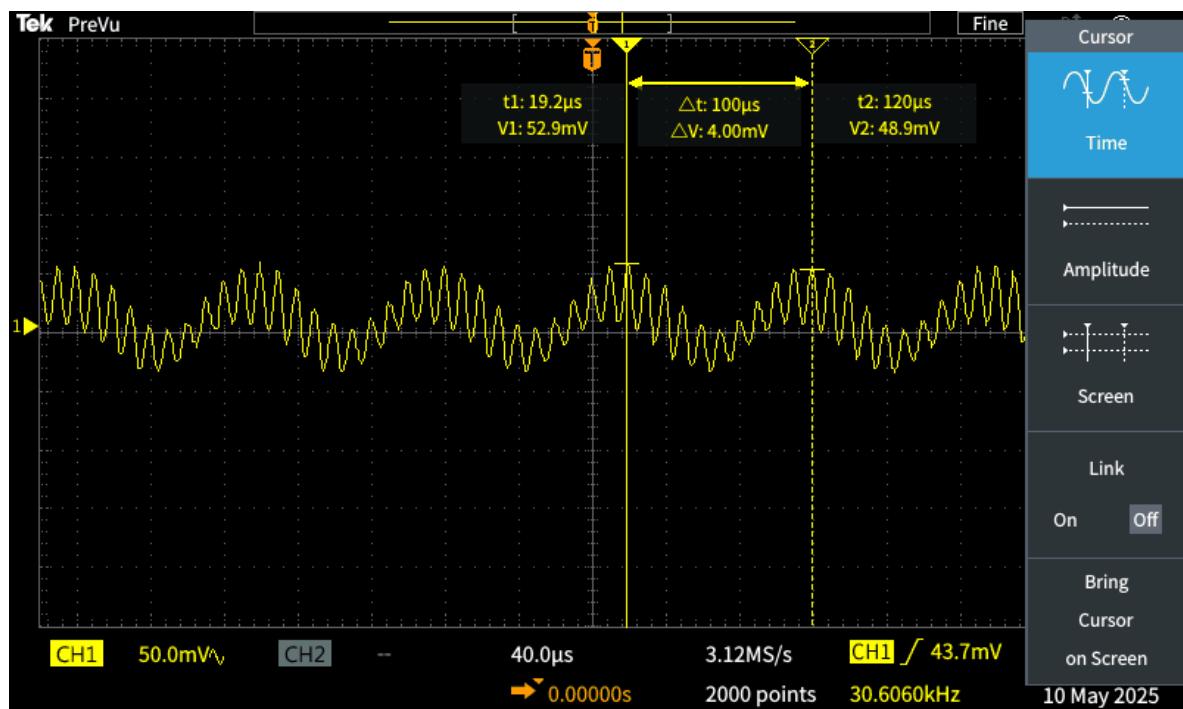
Scope Shot 4 - VRF Period Measured at the Mixer's Output

AFTER THE LAB

For the after the lab portion, it was asked to display screenshots of the FFT function on the oscilloscope with the following different VRF frequencies of 100 kHz, 500 kHz, and 1 MHz. The 100 kHz frequency will not be displayed as it was already displayed above on part 3 of the lab section.

Scope Shot 5 - VRF Frequency of 500 kHz Displaying the 490 kHz and 510 kHz Point

Scope Shot 6 - VRF Frequency of 1 MHz Displaying the 1.01 MHz and 0.99 MHz Point
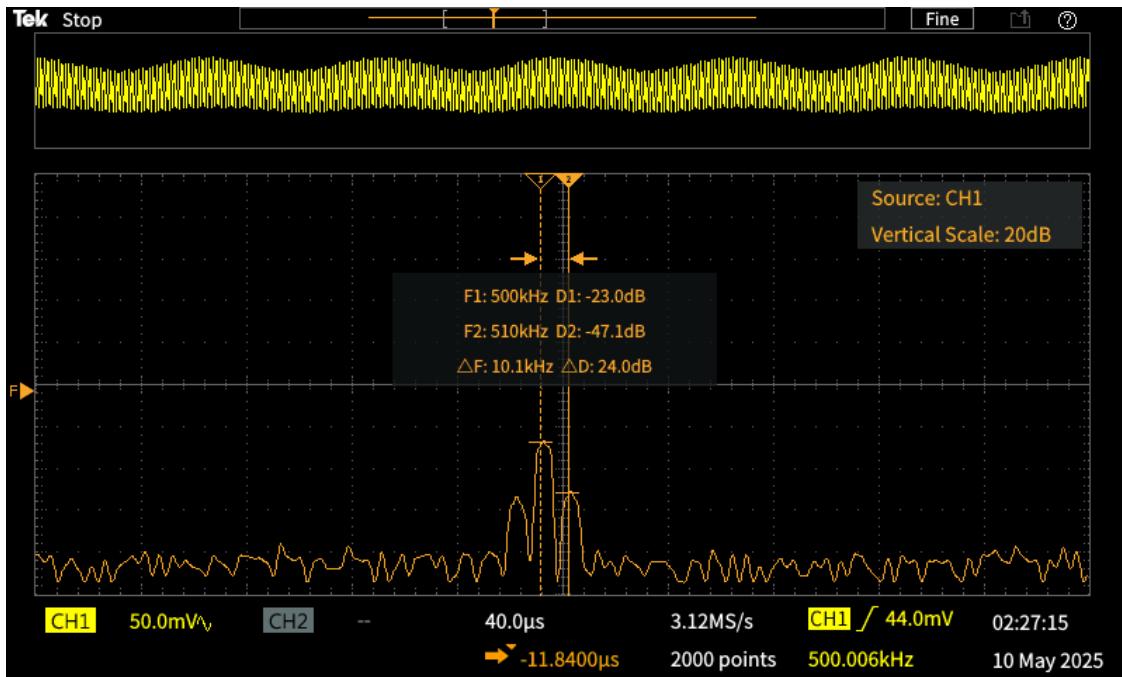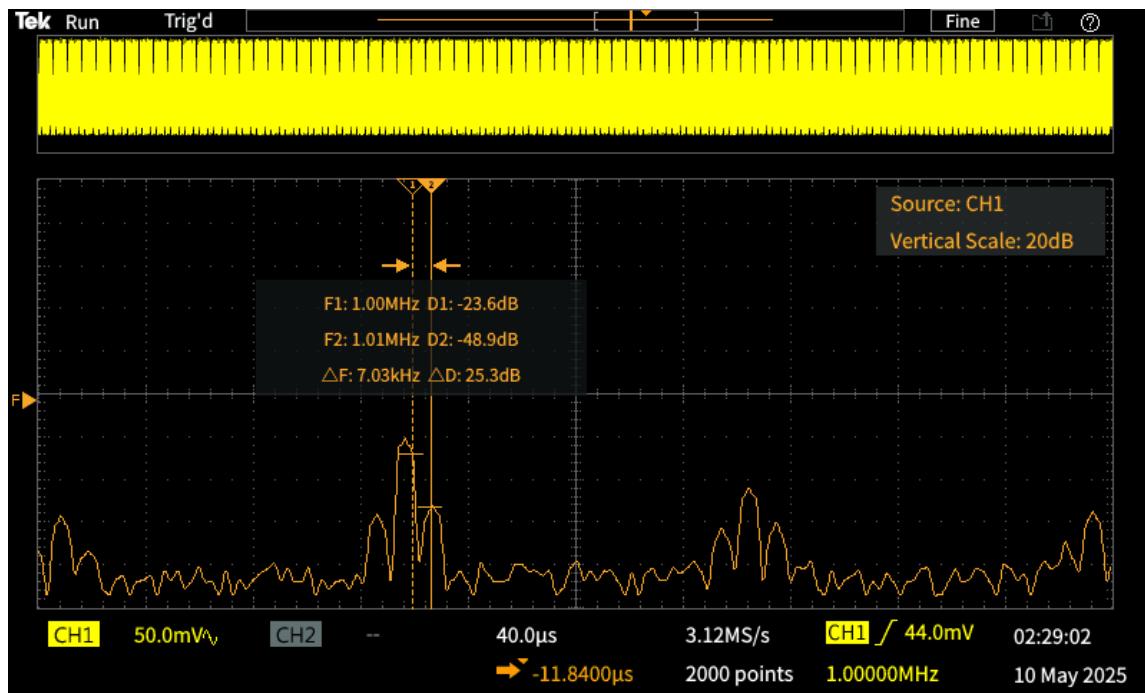
III.   SUMMARY OF RESULTS

Test	Theoretical Value	Simulated Value	Measured Value
BPF Center Frequency	110 kHz	109 kHz	114.5 kHz
BPF Bandwidth	2.2 kHz,	2.3 kHz	4.9 kHz
BPF Quality Factor (Q)	50	47.8	23.4
Tuned Amplifier f_0	110 kHz	123 kHz	126.2 kHz
Tuned Amplifier BW	2.2 kHz	10.2 kHz	12 kHz
Tuned Amplifier Q	50	12.1	10.51
Mixer Frequency Output	frf ± flo	frf ± flo	frf ± flo
Mixer Harmonic Outputs	90, 100, 110 kHz	90, 100, 110 kHz	90, 100, 110 kHz

IV. CONCLUSION

The laboratory experiment successfully demonstrated the design and analysis of fundamental RF circuits. The passive BPF exhibited a measured center frequency of 114.5 kHz, deviating from the designed 110 kHz due to parasitic resistances in the hand-wound inductor and capacitor tolerances. The Q factor of 23.4 was significantly lower than the theoretical 50, highlighting the impact of component non-idealities on high-frequency performance. The tuned amplifier, while functional, showed a reduced Q of 10.51 compared to simulations, likely due to imperfect biasing and additional parasitic capacitances in the MOSFET. The single balanced mixer effectively generated sum and difference frequencies, confirming the principle of frequency mixing.

Critical insights included the importance of accounting for parasitic elements in practical designs, the limitations of idealized simulations, and the challenges of achieving high Q in passive filters with non-ideal components. The experiment also reinforced the utility of FFT analysis in characterizing mixer outputs and the necessity of precise component selection in RF applications. Future improvements could involve using higher-quality inductors with lower DC resistance and automated tuning circuits to enhance stability. Overall, the lab provided valuable hands-on experience in RF circuit design, bridging theoretical concepts with real-world implementation challenges.

University of Texas – Rio Grande Valley
EECE 3225 / EECE 3230
LAB DEMONSTRATION CERTIFICATION

+++

This section to be filled in by project team

Course EECE 3230 Project Lab 6: Part 1

Team Members :

1. Emilio Chavez
2. Jordan Lara
3. _____

Describe what is being demonstrated:

Passive BPF Design and Test Bode Plot, and output wave on oscilloscope.

_____

_____

+++

This section to be filled in by instructor

Signature: _____ Date: 5-7-25 Time: 11:54A

Comments:

$A_{vo} = 1$

$F_c \cong 114k$

If an instructor is not available at demo time, this form can be signed by an EE faculty, teaching assistant, or lab technician. Tape or paste this certification in the lab notebook.

University of Texas – Rio Grande Valley
EECE 3225 / EECE 3230
LAB DEMONSTRATION CERTIFICATION

++

This section to be filled in by project team

Course EECE 3230 Project Lab 6: Part 2

Team Members :

1. Emilio Chavez
2. Jordan Lara
3. _____

Describe what is being demonstrated:

Tuned Amplifier Design and Test Q, 3 dB, BW

++

This section to be filled in by instructor

Signature: _____   Date: 5/14/2025   Time: 12:00 pm

Comments:

If an instructor is not available at demo time, this form can be signed by an EE faculty, teaching assistant, or lab technician. Tape or paste this certification in the lab notebook.

University of Texas – Rio Grande Valley
EECE 3225 / EECE 3230
LAB DEMONSTRATION CERTIFICATION

+++

<u>This section to be filled in by project team</u>

Course EECE 3230 Project Lab 6 : Part 3

Team Members :

1. Emilio Chavez
2. Jordan Lamy
3. _____

Describe what is being demonstrated:

Single Balanced Mixer Sine Wave Message + Carrier.

+++

<u>This section to be filled in by instructor</u>

Signature: Date: Time:
                          5/14/2025   12:02 PM

Comments:

If an instructor is not available at demo time, this form can be signed by an EE faculty, teaching assistant, or lab technician. Tape or paste this certification in the lab notebook.